

Application Note

General Purpose Input/Output Port

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General Purpose Input/Output Port

Introduction

Rockwell's General Purpose Input/Output Port is an interface used to input or output general I/O signals to and from Rockwell decoders. The port's applications range from reading and writing DC-level control signals on a board, to inputting CCIR656 data into the decoder. This application note clarifies the functionality of the GPIO port, including its applications and limitations.

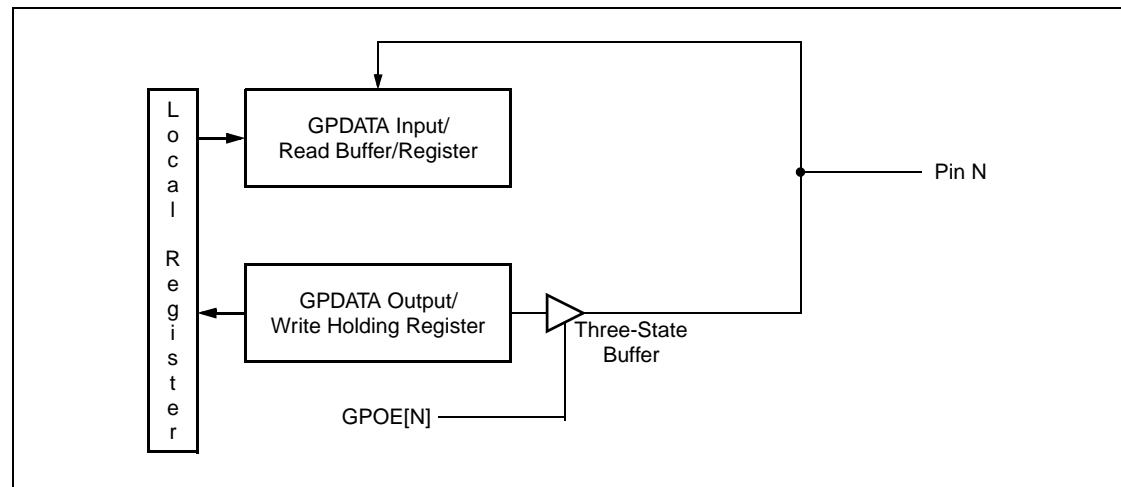
The original concept for the GPIO port was to provide a basic interface. It has since expanded to provide the five interface modes currently available:

- Normal mode
- SPI Input mode
- SPI Output mode
- Digital Video Input mode
- Asynchronous Data Parallel mode

GPIO Pin Architecture

Each GPIO pin is set up as a basic input/output buffer, with each bit of the GPOE register used to enable an individual pin's output driver (refer to Figure 1).

Figure 1. GPIO Pin Architecture



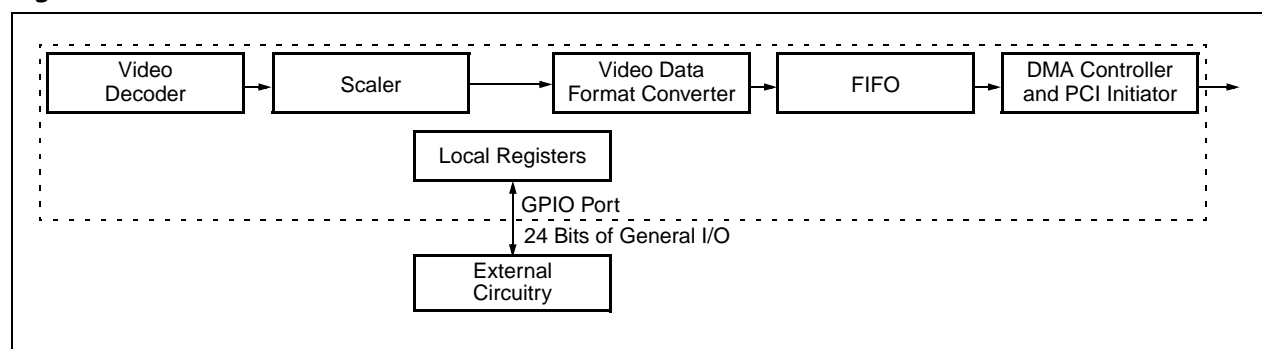
GPIO Modes in Bt848A/878/879

The GPIO port operates in five designated modes: Normal mode, Synchronous Pixel Interface (SPI) Output mode, SPI Input mode, Digital Video Input mode, and Asynchronous Data Parallel mode (Bt878/879 only). The GPIOMODE bits determine the port's mode of operation. Each GPIO pin may be individually configured, but GPIOMODE affects the entire port. The Bt835 GPIO port is distinctly different from the ports on the Bt848A and Bt878/879. Its functionality is discussed in the section on Bt835 GPIO and Digital Video Input over the VD[7:0] Pins.

Normal Mode

The Normal mode of the GPIO port can be used to input or output general board-level signals to or from the PCI interface in the Bt848A/878/879. The GPIOMODE bits are in the default state of “00” during Normal mode. Normal mode is always invoked at power-up, except for the Bt848A when GPWE is sampled high and GPINTR is sampled low upon release of the RST pin. For further details, please refer to the section on Differences Between GPIO in Bt848A and Bt878/879. The GPIO port in Normal mode was not designed to support a high-speed interface for video data or other types of data. The functionality of the GPIO in Normal mode is outlined in Figure 2.

Figure 2. GPIO Normal Mode



Data is written to and read from the GPIO pins through the GPDATA signal. When configured to output signals through the GPIO, information is written to a GPDATA holding register, which is output to the pin. When configured to input data from the GPIO, buffered data is read directly from the pin. Refer to Figure 1.

In the Bt848A only, the option exists to register GPDATA read from the pin, with the separate GPWE signal as a clock. When reading, the GPIE register is used to select between the GPWE registered and simple buffered values. This is detailed in the section on Differences Between GPIO in Bt848A and Bt878/879.

Each GPIO pin must be configured either as an input or an output according to the 24-bit GPOE register. Each bit in the register corresponds to an output driver for a GPIO pin. A value of 1 in the register enables the output buffer, making the pin an output pin. A value of 0 in the register disables the output buffer, making the pin an input pin.

To avoid any conflicts, parts will power-up with the GPOE register set to 0x000000, which means all pins are three-stated and configured as inputs. An exception occurs in the Bt848A, which will power-up in SPI output mode if GPWE is sampled high and GPINTR is sampled low upon release of the RST pin. For further explanation, refer to the section on Differences Between GPIO in Bt848A and Bt878/879.

Any information written to GPDATA[n] while GPOE[n] is low will be lost. Care must be taken not to enable the GPOE bits for GPIO pins, which are set up on the board as input pins. If GPDATA[n] is read while GPOE[n] is enabled, the value read back will echo what was last written to the GPDATA holding register. This will also likely create contention on the signal. Avoid enabling GPOE[n] when expecting to read an external value on GPIO[n].

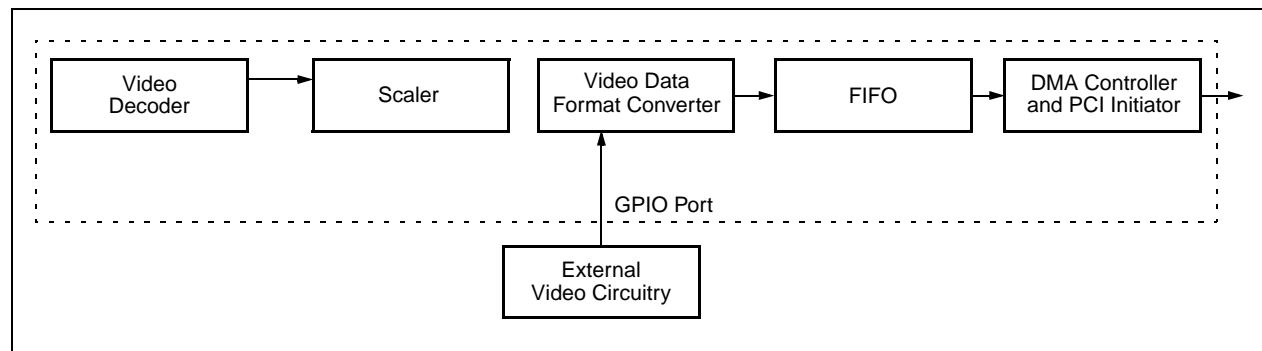
Normal mode permits PCI burst transfers by providing a 64-DWORD contiguous address space. Only the lower 24 bits of the 32-bit PCI DWORD are sent over the GPIO port. An interrupt may be requested through the GPINTR pin. (This pin's functionality is re-mapped to GPIO[8] in the Bt878/879.) The GPINTR pin is linked to the Interrupt Status Register within the part, and controls the GPINT bit of that register. The GPINTI and GPINTC bits provide options for the GPINT bit. The GPINTI bit, when set, inverts the value of the GPINTR signal immediately after the input buffer. The GPINTC bit provides a means of registering the GPINTR input. If the GPINTC bit is low, the GPINTR non-inverted/inverted input will go straight to the GPINT register. If GPINTC is high, the GPINT bit changes on the rising edge of the non-inverted or inverted GPINTR input.

Theoretically, the GPIO port can output (write) at a maximum of 11.1 MHz, and input (read) at a maximum of 8.3 MHz. Normal mode is asynchronous, and it is therefore difficult to ascertain a definite maximum frequency of operation. Real world maximum frequencies will be lower than theoretical frequencies because system configuration and PCI bus availability are limiting factors.

SPI Input Mode

SPI Input mode is used to input Synchronous Pixel Interface video information into the part. The interface accepts 16-bit YCrCb video data. Because the incoming video is inserted after the decoder and scaler, no adjustments can be made on hue, contrast, saturation, or brightness. Similarly, horizontal or vertical filtering or scaling also cannot be performed. Figure 3 demonstrates the architecture of the SPI input mode.

Figure 3. GPIO SPI Input Mode



The GPCLK signal is used to input an external clock signal. The video data and related signals are accepted over the GPIO pins, defined in Table 1.

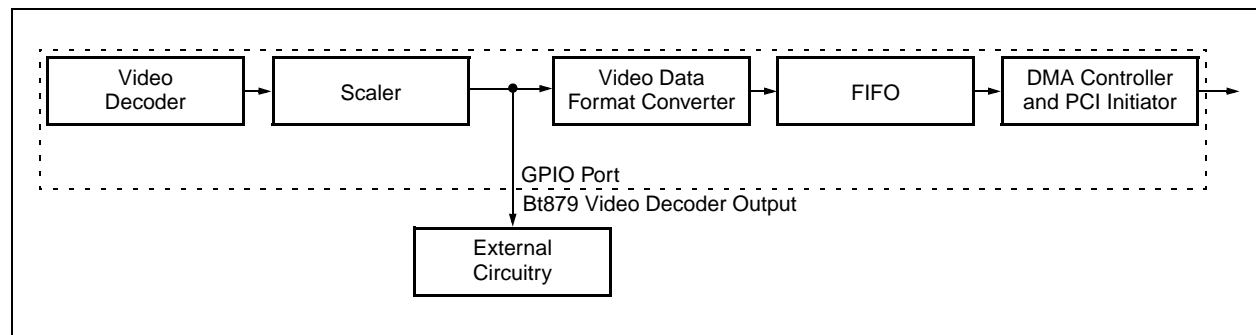
Table 1. Synchronous Pixel Interface (SPI) Input GPIO Signals

GPIO	Signal	Description
[23]	$\overline{\text{HRESET}}$	A 1 to 64-GPCLK-long active low pulse. It is accepted on the rising edge of GPCLK. The falling edge of $\overline{\text{HRESET}}$ indicates the beginning of a new video line.
[22]	$\overline{\text{VRESET}}$	A 1 clock to 6 lines long active low pulse. It is accepted on the rising edge of GPCLK. The falling edge of $\overline{\text{VRESET}}$ indicates the beginning of a new field of video output.
[21]	HACTIVE	An active high signal that indicates the beginning of the active video and is accepted on the rising edge of GPCLK. The HACTIVE flag is used to indicate where nonblanking pixels are present.
[20]	DVALID	An active high pixel qualifier that indicates whether the associated pixel is valid. For continuous valid data, this signal can be connected to HACTIVE or VACTIVE.
[19]	CBFLAG	An active high pulse that indicates when Cb data is being output on the chroma stream. Only required for YCrCb input; otherwise connect to ground.
[18]	FIELD	When high, indicates that an even field (Field 2) is being input; when low, it indicates that an odd field (Field 1) is being output. The transition of FIELD should occur prior to the rising edge of $\overline{\text{VRESET}}$.
[17]	VACTIVE	An active high signal that indicates the beginning of the active video and is accepted on the rising edge of GPCLK. The VACTIVE flag is used to indicate where nonblanking pixels are present.
[16]	GROUND	—
[15:8]	Y[7:0]	Digital pins for the luminance component of the video datastream, or for 8-bit transfers.
[7:0]	CrCb[7:0]	Digital pins for the chrominance component of the video datastream

SPI Output Mode

SPI Output mode is used to output data from the decoder/scaler block of the part. This does not change the regular output of the part. Refer to Figure 4.

Figure 4. GPIO SPI Output Mode



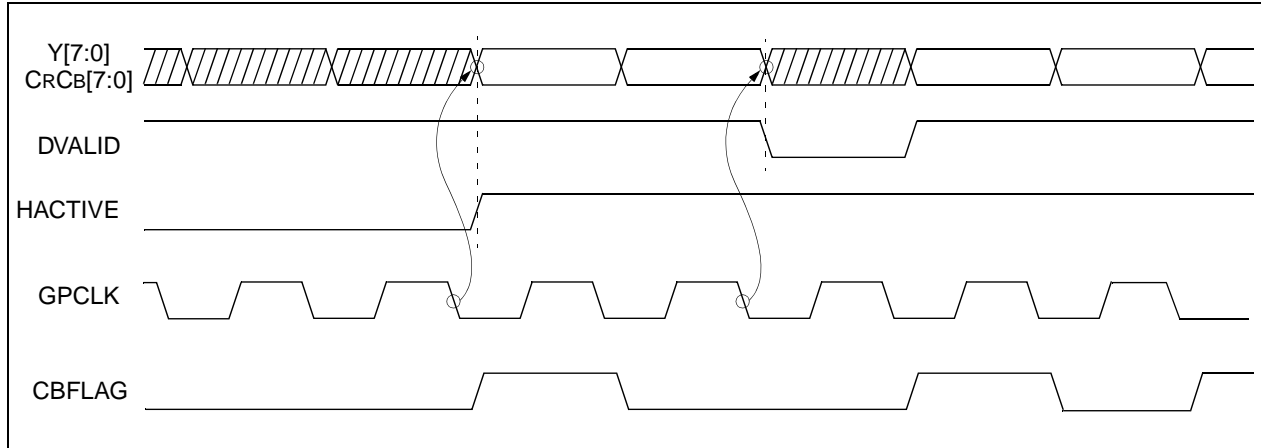
When running the GPIO port in SPI Output mode, the GPCLK is configured to output CLKx1 ($4 * F_{sc}$). CCIR601 is followed when the RANGE bit is set to 0. The GPIO pins are mapped as described in Table 2.

Table 2. Synchronous Pixel Interface (SPI) GPIO Signals

GPIO	Signal	Description
[23]	$\overline{\text{HRESET}}$	A 64-clock-long active low pulse. It is output following the rising edge of CLKx1. The falling edge of $\overline{\text{HRESET}}$ indicates the beginning of a new video line.
[22]	$\overline{\text{VRESET}}$	An active low signal that is at least two lines long (for non-VCR sources, $\overline{\text{VRESET}}$ is normally six lines long). It is output following the rising edge of CLKx1. The falling edge of $\overline{\text{VRESET}}$ indicates the beginning of a new field of video output. The falling edge of $\overline{\text{VRESET}}$ lags the falling edge of $\overline{\text{HRESET}}$ by two clock cycles at the start of an odd field. At the start of even fields, the falling edge of $\overline{\text{VRESET}}$ is in the middle of a scan line, horizontal count $(\text{HPIXEL}/2)+1$, on scan line 263 for NTSC and scan line 313 for PAL.
[21]	HACTIVE	An active high signal that indicates the beginning of the active video and is output following the rising edge of CLKx1. The HACTIVE flag is used to indicate where nonblanking pixels are present. The start and the end of the HACTIVE signal can be adjusted by programming the HDELAY and HACTIVE registers.
[20]	DVALID	An active high pixel qualifier that indicates whether the associated pixel is valid. DVALID is independent of the HACTIVE and VACTIVE signals. DVALID indicates which pixels are valid. DVALID will toggle high outside of the active window, indicating a valid pixel outside the programmed active region.
[19]	CBFLAG	An active high pulse that indicates when Cb data is being output on the chroma stream. During invalid pixels, CBFLAG holds the value of the last valid pixel.
[18]	FIELD	When high, indicates that an even field (Field 2) is being output; when low, it indicates that an odd field (Field 1) is being output. The transition of FIELD is synchronous with the end of active video (i.e. the trailing edge of ACTIVE). The same information can also be derived by latching the $\overline{\text{HRESET}}$ signal with $\overline{\text{VRESET}}$.
[17]	VACTIVE	An active high signal that indicates the beginning of the active video and is output following the rising edge of CLKx1. The VACTIVE flag is used to indicate where nonblanking pixels are present. The start and the end of the VACTIVE signal can be adjusted by programming the VDELAY and VACTIVE registers.
[16]	VBISEL	An active high signal that indicates the beginning and end of the vertical blanking interval. The end of VBISEL will adjust accordingly when VDELAY is changed.
[15:8]	Y[7:0]	Digital pins for the luminance component of the video datastream.
[7:0]	CrCb[7:0]	Digital pins for the chrominance component of the video datastream

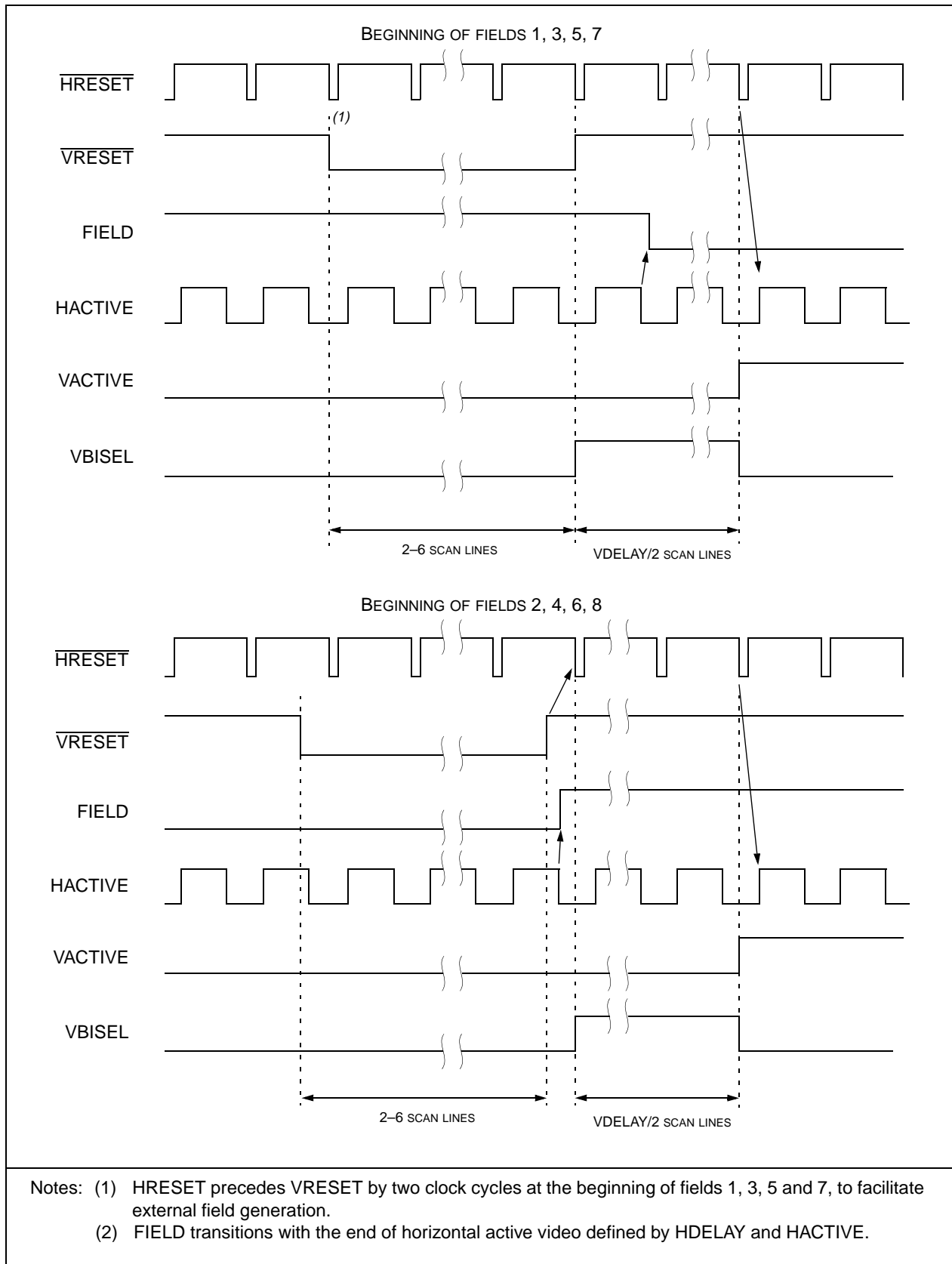
Figure 5 demonstrates SPI output clock-data timing information. The falling edge of the output GPCLK triggers the change in video data. This should allow for ample setup and hold times for any device accepting the data.

Figure 5. Basic Timing Relationships for SPI Output Mode



Related video timing signals for both fields are shown in Figure 6. Note that in Fields 1, 3, 5, and 7 the falling edge of HRESET is two clock cycles ahead of the falling edge of VRESET.

Figure 6. Video Timing in SPI Output Mode



GPIO SPI Mode Timing Parameters

For the timing parameters of GPIO SPI mode, refer to Table 3.

Table 3. GPIO SPI Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
NTSC: 4·F _{SC} Rate	F _{S1}	14.31746	14.31818	14.31889	MHz
PAL: 4·F _{SC} Rate	F _{S1}	17.73358	17.73447	17.73535	MHz
GPCLK Duty Cycle		45		55	%
GPCLK (falling edge) to Data Delay	4	0		15	ns
Data/Control Setup to GPCLK (falling edge)	5	5			ns
Data/Control Hold to GPCLK (falling edge)	6	5			ns
GPCLK Input:					
Cycle Time	7	56		10,000	ns
Low Time	8	22			ns
High Time	9	22			ns

Digital Video Input Mode

The GPIO port can be configured to accept general digital datastreams. The parts contain a TG_RAM-based state machine that isolates the digital video input events from the internal decoder timing. This allows the digital video input H & V events to synchronize the sequencer, and allows the programmable output events to be positioned where needed to synchronize the decoder.

The digital input port provides flexibility for interfacing to various video standards. Software for programming the parts is included in the development kit for interfacing to the supported video standards. Table 4 provides the alternate pin definitions when using the digital video-in mode. Additional digital interfaces may be implemented by changing the TG_RAM contents. Contact your local Rockwell sales office for more information.

Table 4. Pin Definition of GPIO Port When Using Digital Video-In Mode

GPIO	Signal	Description	Pin Number
[23]	CLKx1	Output signals for synchronizing to input video.	56
[22]	FIELD		57
[21]	VACTIVE		58
[20]	VSYNC		59
[19]	HACTIVE		60
[18]	HSYNC		61
[17]	Composite ACTIVE		67
[16]	Composite SYNC		68
[20]	VSYNC/FIELD	Input signals for synchronizing to input video.	59
[18]	HSYNC		61
[7:0]	DATA	Cb0, Y0, Cr0, Y1, ... Video data input at GPCLK = CLKx2 rate.	86–79

CCIR656

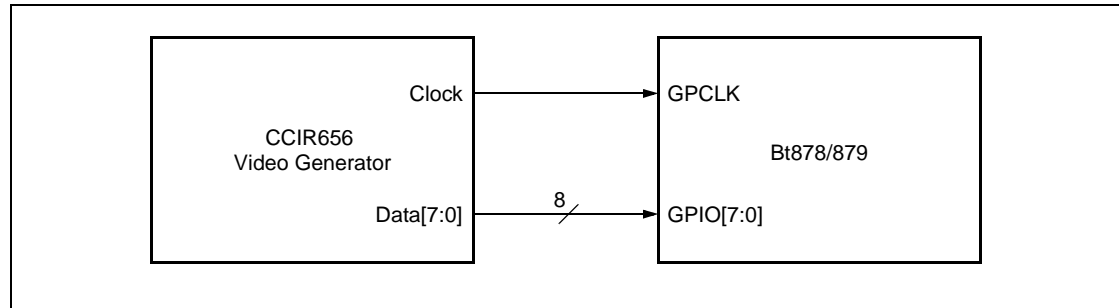
CCIR656 is a 27 MB/s interface in the form of Cb, Y, Cr, Y, Cb, etc. In this sequence, the word sequence Cb, Y, Cr, refers to co-sited and color-difference samples, and the following word, Y, corresponds to the next luminance sample.

In this interface, two timing reference codes, SAV and EAV, occur at the start and end of active video, respectively. These 4-byte codes occur at the outside boundaries of the active video. 720 pixels in the active video line correspond to 1440 samples. 1448 bytes comprise a video data block (one line of video with reference codes).

The full video line consists of 1716 bytes (in 525 line systems) and 1728 bytes (in 625 line systems). The line is broken into two parts. The first part is blanking, which consists of the front porch, HSYNC, and back porch, 276 bytes (288 in 635 line systems) from EAV through SAV. The leading edge of HSYNC occurs 32 bytes (24 in 625 line systems) after the start of the digital line. The field interval is aligned to this leading edge of HSYNC.

See Figure 7 for a diagram of the interface. For a full reference on this standard, please refer to the International Telecommunications Union (ITU) specification, ITU-R-BT656. This can be obtained from the ITU Web Site at <http://www.itu.int/publications/>.

Figure 7. CCIR656 Interface to Digital Input Port



Modified SMPTE-125

The Modified SMPTE-125 interface is the same as CCIR656, but the clock runs at 24.54 MHz, with 640 active pixels on a 780 pixel line. This clock rate difference provides simple interface for digital cameras from Silicon Vision and Logitech.

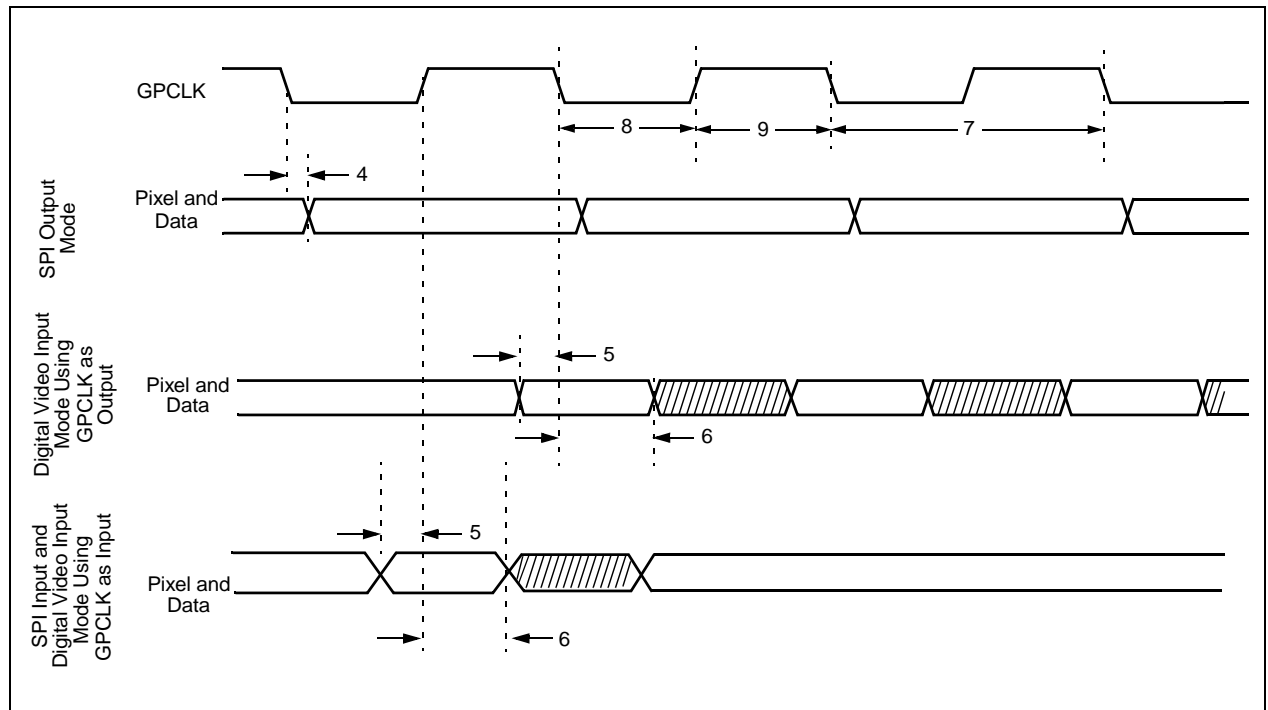
To properly implement a digital video input mode with CCIR656 incoming data, several steps must be taken to set the part up to accept data:

1. Set the signal format to CCIR656 (VSFMT[2:0] in the DVSIF register).
2. Set the sync video reference to align with Cb, Cr, Y1, or Y0 (SVREF bits in DVSIF register).
3. Disable the sync output register (VSIF-ESO in the DVSIF register).
4. Load the TG_RAM table. Place the Timing Generator Video Mode into Read/Write mode (TGC_VM bit in the TGCNTRL register). Reset the Timing Generator Address (GPC_AR in the TGCNTRL register). Write the LSB of the TG_RAM table first. The address will be incremented automatically. TG_RAM maps may be obtained from your local FAE.
5. Set the desired PLL frequency. (This is not necessary, but will provide the correct bluescreen output in the event the input is disconnected. If the input clock is disconnected, the decoder will run off the PLL, or the XTAL if the PLL is sleeping.)
6. Select GPCLK as the decoder input clock. Set the GPIO_DMA_CTL register bits [12:10] to 100 to select the SPI Input mode. The entire decoder will now be run by the external clock.
7. Enable the Timing Generator Video mode, by setting bit 0 of the TGCTRL register to a logical 1.

GPIO Timing Diagram for SPI and Digital Video Input Modes

Figure 8 provides an overview of the GPIO timing for SPI Input and Digital Video Input modes.

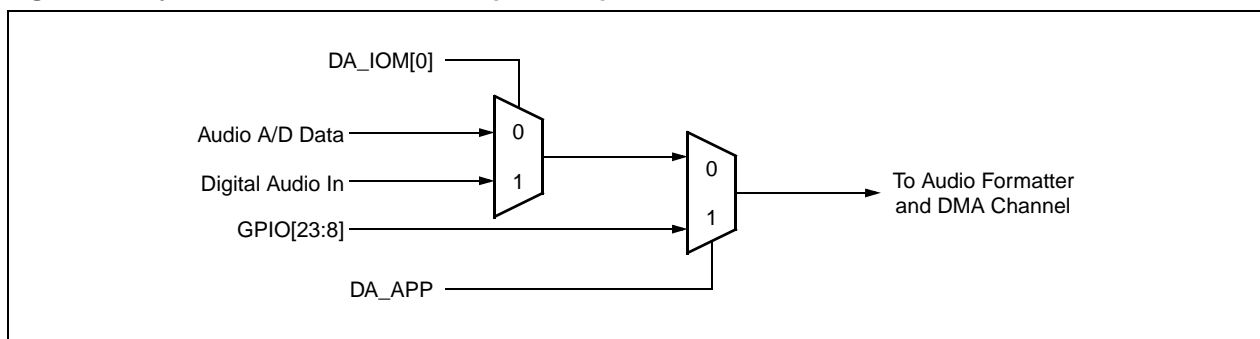
Figure 8. GPIO Timing Diagram



Asynchronous Data Parallel Mode: Raw Data Capture (878/879 only)

The asynchronous data parallel port interface allows the user to multiplex raw data from the GPIO port into the audio packetizer. Normally, the audio processor selects the 16-bit digitized analog data from the audio A/D and from the 16-bit digital audio input data. By setting the DA_APP bit in Bit 5 of the Audio Control Register (0x10C), the user may configure the part to disregard the 16-bit digital audio data, and use the information on GPIO [23:8]. Setting the DA_APP bit overrides the DA_IOM bit, as shown in Figure 9.

Figure 9. Asynchronous Data Parallel Input Multiplexer Block



When the DA_APP bit is set, the GPIOMODE bits are overridden, and the GPIO will always go into Asynchronous Data Parallel mode. The DA_APP bit also switches the functionality of the ALRCK pin. When DA_APP is high, ALRCK should be used to clock in the data on GPIO [23:8]. This interface is dubbed “asynchronous,” because the clock is not required to be continuous or fixed-rate. From the point where it is multiplexed into the Digital Audio Packetizer, the GPIO data is treated the same as normal audio data. From the Packetizer, the data goes into a 35×36 FIFO, and from the FIFO, to the PCI initiator. Because of the mode’s asynchronous configuration and system-to-system variations in PCI bus availability, it is difficult to specify a maximum operating frequency.

As in Normal mode when reading, the theoretical maximum frequency of 8.3 MHz will likely never be achieved in a real-world system.

Differences Between GPIO in Bt848A and Bt878/879

Several key differences exist between the GPIO ports in the Bt848A and the Bt878/879. The Bt848A provides the option to register the GPIO input data with the GPWE signal. The Bt878/879 eliminates this option, thereby eliminating the GPWE pin and the 24-bit GPIE register. Only the direct buffered input may be read in the Bt878/879.

There is no dedicated GPINTR pin on the Bt878/879. This pin’s functionality has been remapped to share the GPIO[8] pin. The interrupt function may be invoked in Normal mode when GPOE[8] is low.

The Bt848A provides a default option to configure the GPIO in SPI-16 Output mode by sampling GPWE high and GPINTR low at the release of the RST pin. This option does not exist in the Bt878/879.

The Bt848A automatically enables the GPIO outputs during SPI Output mode; the Bt878/879 does not. Therefore, the GPOE outputs in the Bt878/879 must be properly set for SPI Output mode to work.

The Bt878/879 digital video input mode input syncs are re-mapped to the same signals as the output mode. GPIO[20] and GPIO[18] serve as both input/outputs for VSYNC and HSYNC signals, respectively.

The Bt848A's GPX[5:0] pins are not present on the Bt878/879.

Bt835 GPIO and Digital Video Input over the VD[7:0] Pins

The GPIO on the Bt835 operates only in Normal mode. Because the Bt835 has no PCI interface, its GPIO is limited by the speed of the I2C bus, which is in the 100KHz range. This, coupled with the asynchronous nature of the GPIO, makes the Bt835 GPIO particularly unsuitable for high speed data transfer. It is, however, still very useful for reading and writing board-level DC signals.

Users may wish to input a digital CCIR656 datastream to the Bt835. This is not done via the GPIO pins, as it is in the PCI decoders. To do this, the appropriate bits in the VSIF and TG_CTL registers must be selected. The incoming 8-bit digital video should be input on the VD[7:0] pins. As in the PCI parts, running the part using an external 27 MHz clock requires the user to program and enable the Timing Generator RAM. Several steps must be followed to properly write the Bt835 TG_RAM and to enable Timing Generator mode:

1. Verify that TGEN, register 0x24 bit 5, is in Read/Write mode (set to 0).
2. Reset TG_RAM address, register 0x24, bit 4. Toggle this bit from low to high, and then back to low.
3. Write to the TG_RAM continuously, starting by placing the first value in register 0x40.
4. Reset TG_RAM address, register 0x24, bit 4. Toggle from low to high to low.
5. Place the part in Timing Generator mode by setting the TGEN, register 0x24, bit 5 (set to 1).

This sequence must be followed when a switch is made from the composite input to a 27 MHz digital input. To switch back to the composite input, the TGEN must be set back to Read/Write mode, and the appropriate clock source must be selected in the TGCKI[1:0] bits.

TG_RAM maps for the Bt835 are the same as those used in the PCI parts, and should be obtained from your local FAE. These maps should be loaded into the Bt835 TG_RAM, starting at register address 0x40. It is important that when loading the TG_RAM, the load is continuous. In other words, do not load a part of the RAM, then access other registers, and then try to resume loading the RAM.